The purpose of this template is to provide guidance to vendors on the information the CTS-2 benchmark teams wants to understand about the test environment benchmarking runs were performed on. Not all the information in this document may apply to your tests, and if there is important information missing from this document that you believe will help the review team in evaluating your work you are encouraged to submit that information as well.

**FOMs**

|  |  |  |
| --- | --- | --- |
| **Benchmark** | **CTS-1 FOM** | **Projection** |
| **HPCG** | 7.56786112 |  |
| **LAGHOS** | 190.272 |  |
| **Quicksilver** | 2.131e+07 |  |
| **SNAP** | 1.68 |  |

**Machine/Simulator Environment**

In this section describe the general test environment experiments were run on. We expect the same general environment, e.g. processor, memory, BIOS, etc. will be used for all projections for a single device. If different configurations are used to project different applications these details will be called out in the individual code sections and the reasoning for why the changes are made should be provided. Any changes made to improve performance that would not be possible in production, e.g. rebooting nodes between application runs, will be discounted in the evaluation.

**HW Environment**

1. Processor make and model (or name)
2. Processor Thermal Design Point (TDP)
3. Number of processor sockets per node
4. Number of cores per processor
5. Number of threads per core
6. Core base frequency
7. Core max (turbo) frequency
8. Number, width and clock of SIMD units
9. Clock/width/bandwidth and type of interconnection network (e.g., 20 bi-di lanes, 9.6 GHz, QPI, Hypertransport)
10. Number of memory channels per processor socket
11. Number of DIMMs per memory channel (or equivalent)
12. Type, speed and capacity of memory (e.g., 16GB DIMMs of 3200 MHz DDR5)
13. Width of memory data lanes, if different from standard DIMMs (8 bytes)
14. Column Address Select (CAS) latency of memory, in nanoseconds or in memory clocks

**BIOS Settings**

1. Processor variable frequency (e.g., TurboBoost) enabled/disabled
2. Number of threads enabled per core
3. Integrated Memory Controller interleave policy (e.g., 1-way, 2-way, etc.)
4. DRAM Page Policy (e.g., Open, Closed, Adaptive)
5. LLC Prefetch enabled/disabled
6. Energy efficiency settings that are enabled/disabled

**Noise Mitigation Resources**

All current CTS systems use techniques to mitigate system noise and we expect future ones will too. All benchmark runs should provision hardware resources for noise mitigation. Current systems leave the hyper-threads free for this purpose, but core specialization may be used in the future. If core specialization is used at least two cores should be used for mitigation.

1. Noise mitigation hardware left free:

**Code Build Summary:**

For the applications please document the following build and run information.

**HPCG:**

Compiler:

Flags:

MPI ranks:

OpenMP Threads per MPI Rank:

Changes to the machine/simulator environment from above:

**Laghos:**

Compiler:

Flags:

MPI ranks:

OpenMP Threads per MPI Rank:

Changes to the machine/simulator environment from above:

**Quicksilver:**

Compiler:

Flags:

MPI ranks:

OpenMP Threads per MPI Rank:

Changes to the machine/simulator environment from above:

**Snap:**

Compiler:

Flags:

MPI ranks:

OpenMP Threads per MPI Rank:

Changes to the machine/simulator environment from above:

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